

FIG. 1A (PRIOR ART)

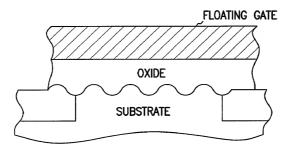


FIG. 1B (PRIOR ART)

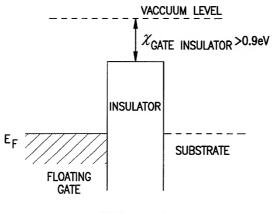


FIG. 1C (PRIOR ART)

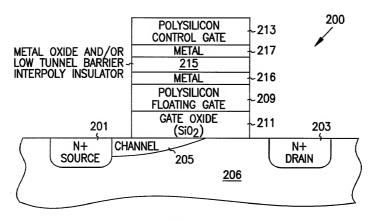
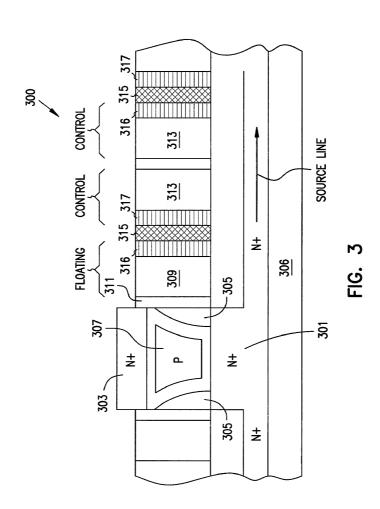
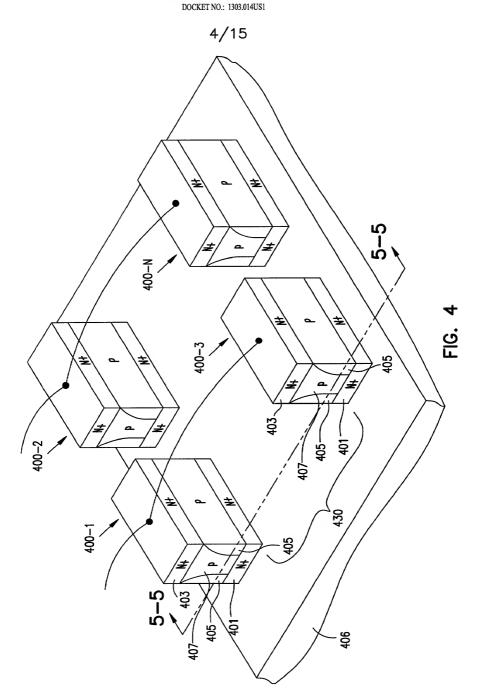
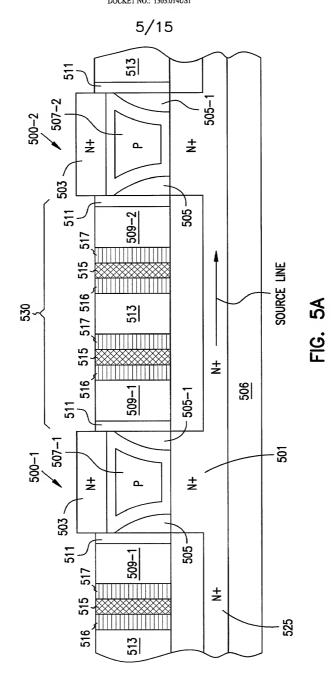
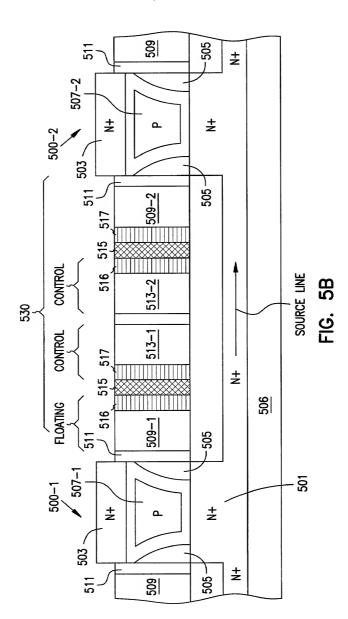


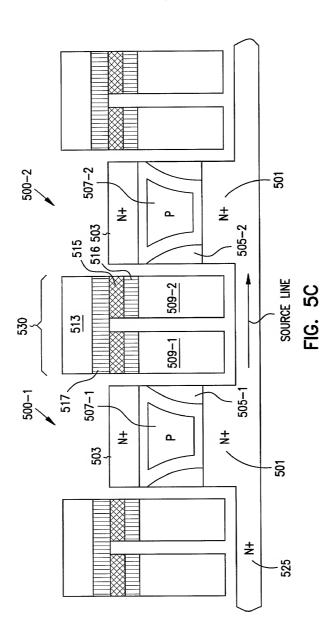
FIG. 2

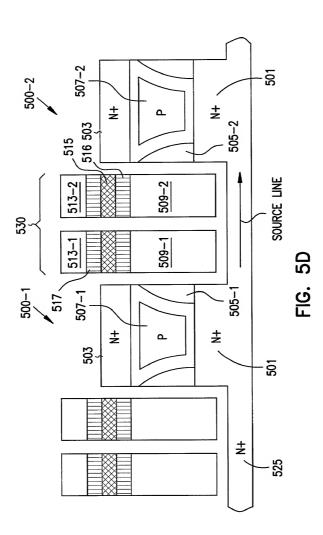


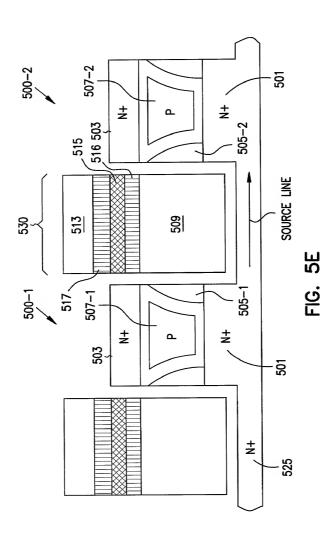


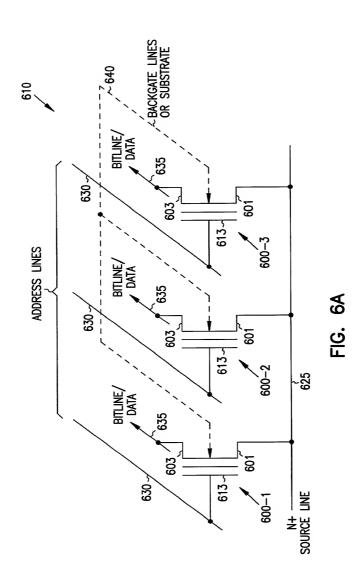












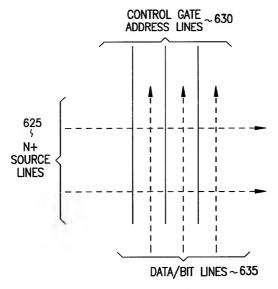
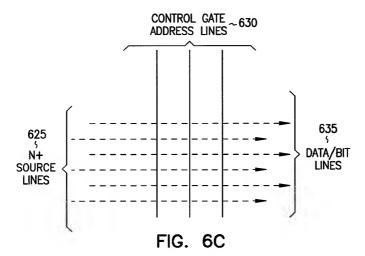
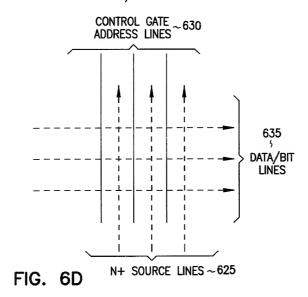


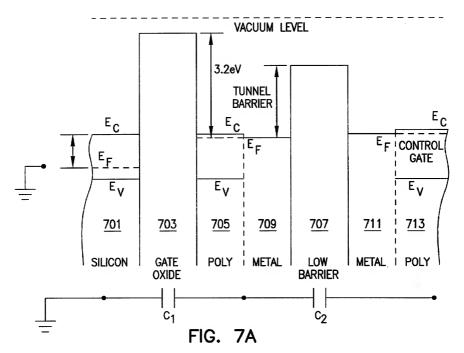
FIG. 6B



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TITLE; FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS





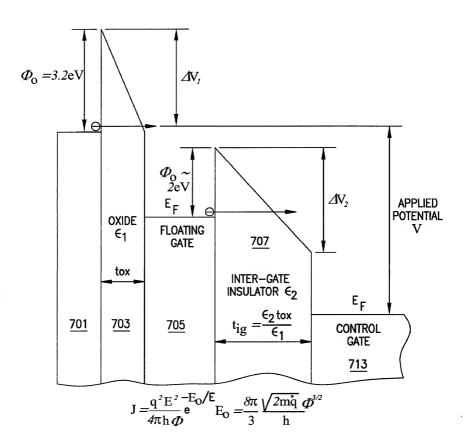


FIG. 7B

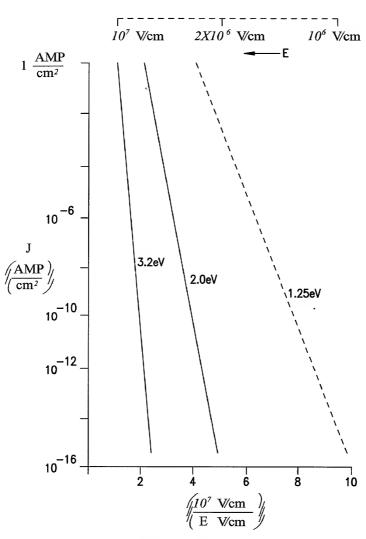


FIG. 7C

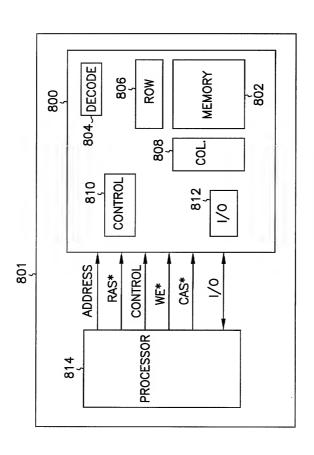


FIG. 8